Huizhou LCDind Technology Co., Ltd.

PRODUCT SPECIFICATION

MODEL NAME: **DBC051LCDAFN50R050A**

Date: 2020/11/16

Version: DRAFT

Preliminary Specification

□ **Final Specification**

FOR CUSTOMER	
CUSTOMER APPROVED	

PREPARED BY	CHECKED BY	APPROVED BY	DATE

Contents

Revision History

Version	Content	Page	Date
	First Release		

A. General Description

DBC051LCDAFN50R050A is an a-Si & transmissive type Thin Film Transistor Liquid crystal Display (TFT-LCD) with AHVA (Advanced Hyper View Angle) technology. This model is composed of a TFT-LCD, a driver, an FPC (flexible printed circuit), and a backlight unit. TCON (timing controller) is also embedded in source driver.

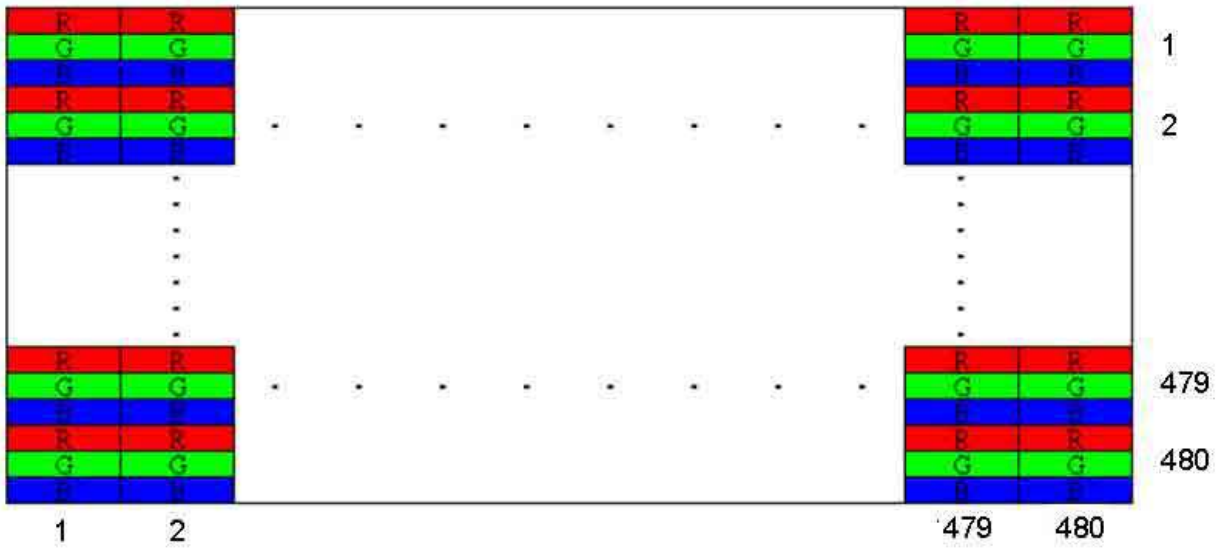
B. Features

- 5.1-inch (1:1) display, cutted from 7" 800*480 LCD.
- 480 x 480RGB resolution in RGB horizontal stripe arrangement
- Interfaces: parallel RGB 24-bit
- Advanced Hyper View Angle – Normal Black wide view technology
- RoHs compliance

C. Physical Specifications

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	480 (H)×480 RGB(V)	
2	Active Area	mm	91.44(H)×91.44(V)	
3	Screen Size	inch	5.1(Diagonal)	
4	Dot Pitch	mm	0.1905(H)x0.0635xRGB(V)	
5	Color Configuration	--	R. G. B. Horizontal Stripe	Note 1
6	Color Depth	--	16.7M Colors	
7	Overall Dimension	mm	106.0(H) × 106.0(V) × 4.5(T)	Note 2
8	Weight	g	TBD	
9	Display Mode	--	Normally Black	
10	LCD Surface Treatment		AG	

Note 1: Below figure shows horizontal stripe arrangement.

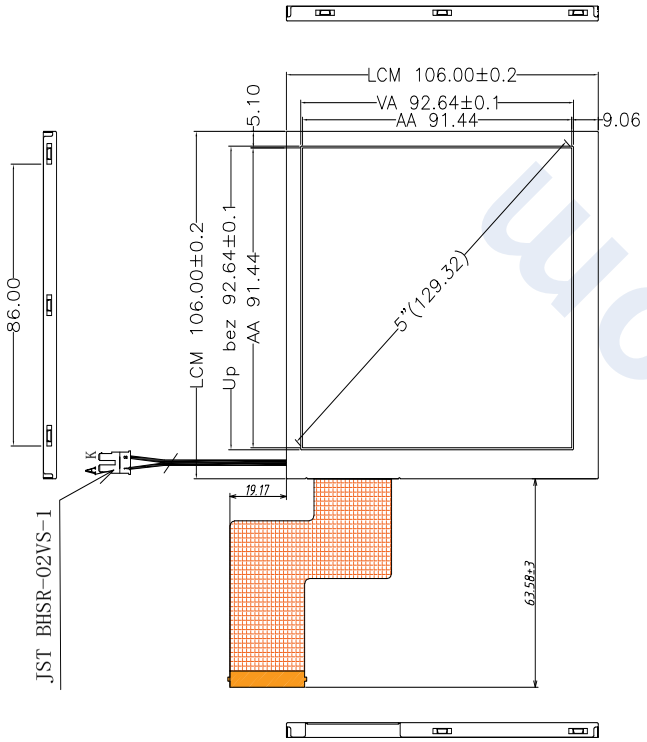


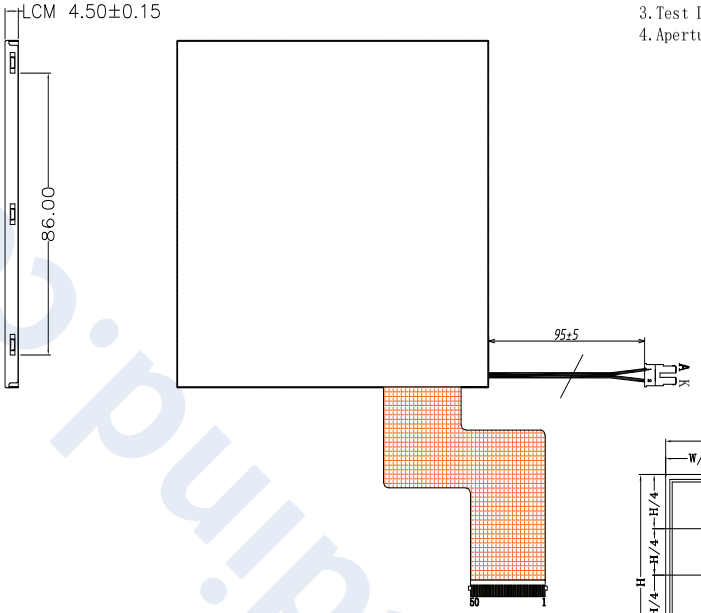
Note 2: including FPC. Please refer to the drawing in page 6 for further information.

第三视角

RoHS 产品

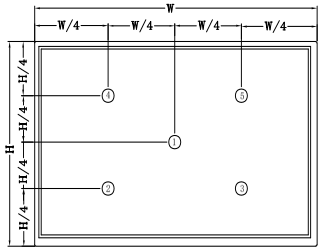
ISSUE	DATE	DESCRIPTION	REVISER
0	20200826	首次发行	夏雷





4. Test Point(测试点):

1. Environment Luminance(环境亮度):≤0.1cd/m2
2. Test Instrument(测试仪器):BM-7
3. Test Distance(测试距离):500 mm
4. Aperture Diameter(光圈直径):07.7(1°)



5点测试示意图

1.Mechanical Outline (Unspecified Tolerances is ± 0.3mm)

2.Electrical-Optical Characteristics (Ta=25°C)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forward Voltage	VF		9.0	10.2	V	定电流 IF=120mA
Dominant Wave Length	X	0.28	0.35	0.41		
	Y	0.32	0.36	0.42		
Uniformity	Avg	70			%	
Module Luminance	Lv	600	700		cd/m²	

•Operating Temperature: -20~+70°C•Storage Temperature:-30~+80°C

TYPE	TFT液晶模组	DITENG MODE	DBC05LCD1AFN50R050A		
CUSTOM NO	KH057	EDITION	A2	DATE	20200826
CUSTOM MODEL	5.0 480×480	UNIT	MM	APPROVED	
CUST Drawing		SCALE	1:1	CHECK	
		PAGE	1/1	DESIGNED	

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E. Electrical Specifications

1. Pin Assignment

a. Main FPC

Connector = HIROSE,FH52-50S-0.5SH

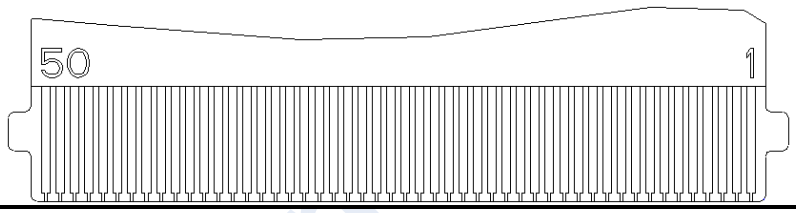
No.	Pin Name	I/O	Description	Remarks
1	CS	I	SPI signal	Note 1
2	SCL	I	SPI signal	Note 1
3	SDO	O	SPI signal	Note 1
4	SDA	I	SPI signal	Note 1
5	VCOM	P	Common electrode driving voltage	
6	UPDN	I	Vertical scan direction control. “H”→ Down to Up; “L”→ Up to Down	Note 2
7	SHLR	I	Horizontal scan direction control. “H”→ Left to Right; “L”→ Right to Left	Note 2
8	AVDD	P	Power for analog	
9	GND	-	Ground	
10	VDD	P	Power for Logic	
11	VDD	P	Power for Logic	
12	RSTB	I	Reset	
13	MODE	I	HV or DE selection	Note 3
14	DR0	I	Red Data0	
15	DR1	I	Red Data1	
16	DR2	I	Red Data2	
17	DR3	I	Red Data3	
18	DR4	I	Red Data4	
19	DR5	I	Red Data5	
20	DR6	I	Red Data6	
21	DR7	I	Red Data7	
22	DG0	I	Green Data0	
23	DG1	I	Green Data1	
24	DG2	I	Green Data2	
25	DG3	I	Green Data3	
26	DG4	I	Green Data4	
27	DG5	I	Green Data5	
28	DG6	I	Green Data6	
29	DG7	I	Green Data7	
30	DB0	I	Blue Data0	
31	DB1	I	Blue Data1	
32	DB2	I	Blue Data2	
33	DB3	I	Blue Data3	
34	DB4	I	Blue Data4	
35	DB5	I	Blue Data5	
36	DB6	I	Blue Data6	
37	DB7	I	Blue Data7	

38	GND	-	Ground	
39	DCLK	I	Clock For Input Data	
40	GND	-	Ground	
41	DE	I	Data Input Enable	
42	HS	I	Horizontal Sync	
43	VS	I	Vertical Sync	
44	NC	-	No Connect	
45	VGH	P	Positive power supply voltage for Gate driver	
46	NC	-	No Connect	
47	VGL	P	Negative power supply voltage for Gate driver	
48	NC	-	No Connect	
49	INV2B	I	2-Frame polarity inversion. Normally pull ‘’High’’ ‘’High’’: Disable (Default) , ‘’Low’’: Enable , change 1-frame to 2-frame inversion	
50	GND	-	Ground	

I: Digital signal input, O: Digital signal output, P: Power input

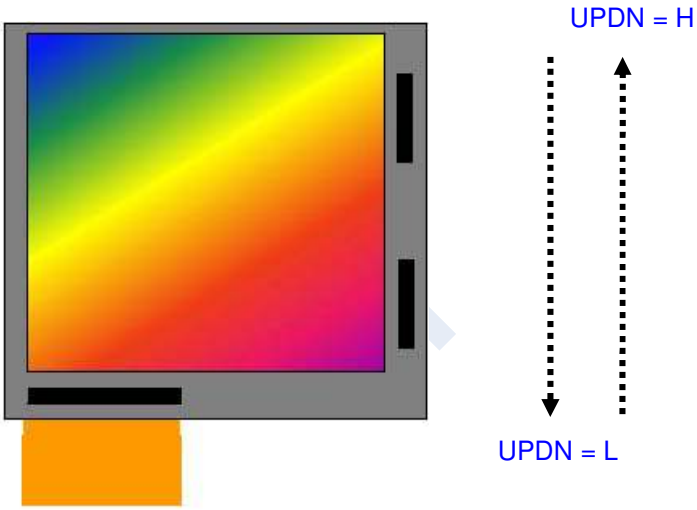
Main FPC Pin1 position: Please refer to the drawing in page 6

Gold finger on TOP:



Note 1: CS, SCL, SDO and SDA are SPI signals. If SPI is used, please refer to section 5.1 ;
if not, that can be floating.

Note 2:



Note 3: MODE = ”H”, the timing format is HV mode; MODE = ”L”, the timing format is DE mode.

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Supply Voltage	VDD	-0.3	4.5	V	Note 1
Analog Input Voltage	AVDD	-0.5	15	V	Note 1
Gate Driver Voltage	VGH-VGL	-0.3	40	V	
	VGL	-20	0.3		
LED Power Consumption		3.5	4.8	W	
Storage Temperature	T_{ST}	-20	+70	℃	
Operating Temperature	T_{OP}	-10	+60	℃	

Note 1: Functional operation should be restricted under ambient temperature (25

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

3. DC Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

a. Power Specification

Operating Voltage

Parameter	Symbol	Min	Typ.	Max.	Unit	Notes
Power Supply	VDD	3.0	3.3	3.6	V	
	AVDD	12.5	13	13.5	V	
	VGH	19.5	20	20.5	V	
	VGL	-8.5	-8	-7.5	V	
	VCOM	-	4.65	-	V	(Tentative)
Input Signal Voltage	Vref(V1~V9)	0.4*AVDD	-	AVDD-0.3	V	
	Vref(V10~V18)	0.3	-	0.6*AVDD	V	
Input high voltage	Vh	0.7*VDD	-	VDD	V	
Input low voltage	Vl	GND	-	0.3*VDD	V	

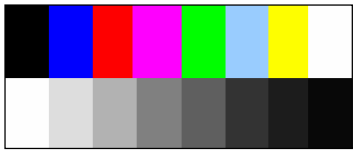
b. Panel Loading

(Tentative)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Panel current	IVDD	14	14.2	15	mA	Note 1
	IAVDD	22	22.5	40	mA	
	IVGH	1.15	1.17	1.18	mA	
	IVGL	1.05	1.07	1.08	mA	
	IVcom	0.02	0.02	0.03	mA	

*** The limitation range of Minima and Maxima is derived base on operating at ambient temp 25˚C
All conditions should be set typical value.
The panel can operate normally in the recommended operating condition.
Need to fine tune the best value from Vcom range for performance

Note 1 :Typical current test pattern.
Panel loading for power reference.



c. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Supply Current	I_L	-	20	35	mA	Per string Note1
LED Supply Voltage	V_L		9.0	10.2	V	Note 1 & 2 , 25° C
LED Life Time	L_L	15000	---	---	Hr	Note 3

: The LED lifetime 10000hrs means: after 10000hrs normally use at 20mA, under +25

*** LED backlight is composed by total18 LEDs (6 strings, 3pcs per string).

Note 1: The LED backlight supply power is for 6 strings of LEDs.
Note 2: The voltage capacity of LED driver IC must be over the max of LED Supply Voltage condition.
Note 3: The LED lifetime 10000hrs means: after 10000hrs normally use at 80mA, under +25° C, the brightness decreases to 70% of original level.
Note 4: Thermistor type: MURATA - NCP15WF104F0SRC.

d. Recommend Gamma 2.2 Voltage

(Tentative)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Gamma Voltage	V1	-	12.36	-	V	
	V2	-	11.92	-	V	
	V3	-	10.39	-	V	
	V4	-	9.82	-	V	
	V5	-	9.16	-	V	
	V6	-	8.54	-	V	
	V7	-	8.11	-	V	
	V8	-	6.97	-	V	
	V9	-	6.86	-	V	
	V10	-	6.06	-	V	
	V11	-	5.95	-	V	
	V12	-	4.84	-	V	
	V13	-	4.39	-	V	
	V14	-	3.82	-	V	
	V15	-	3.21	-	V	
	V16	-	2.72	-	V	
	V17	-	1.33	-	V	
	V18	-	0.80	-	V	

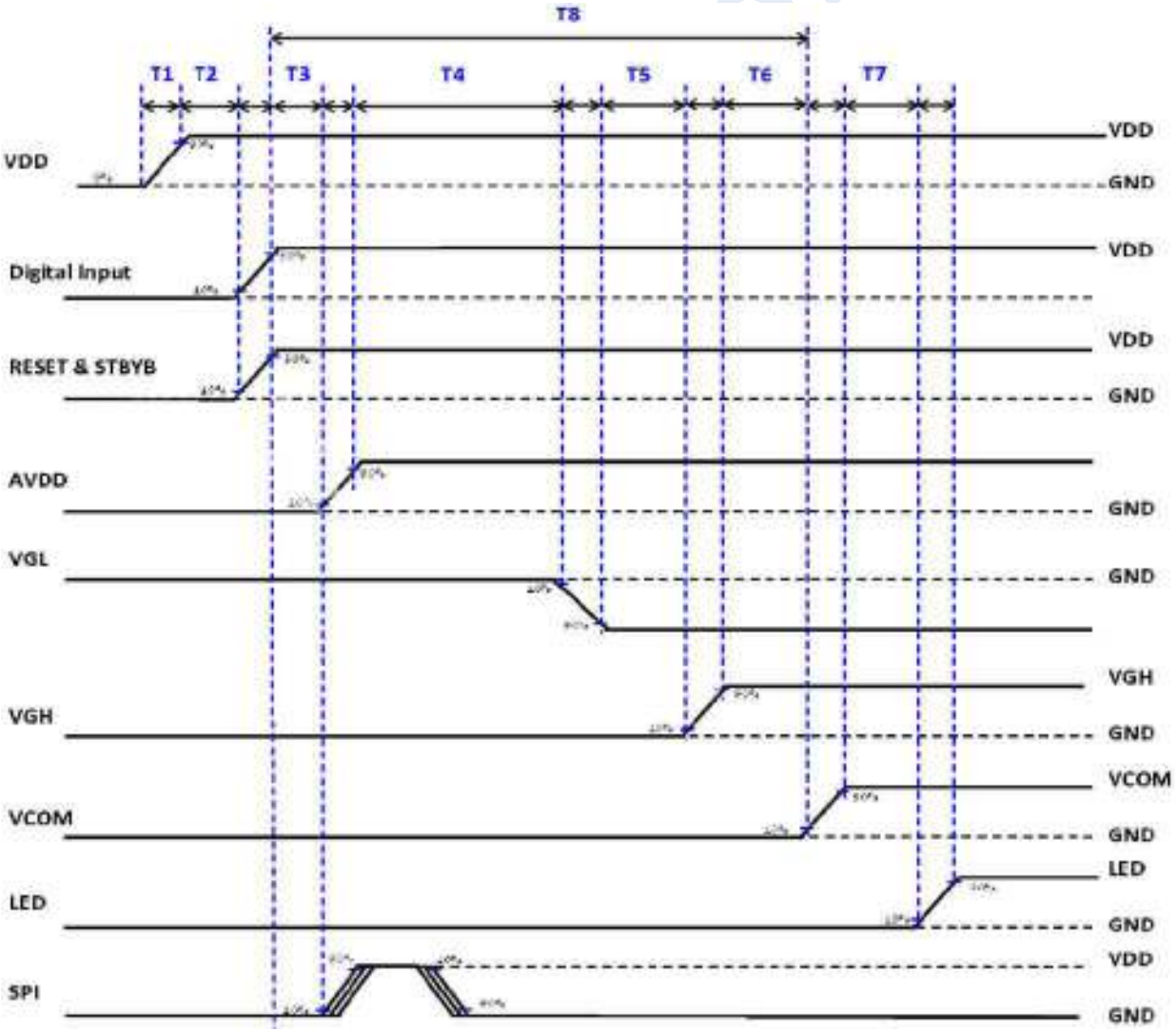
4. AC Electrical Characteristics

a. Power on/off sequence

The LCD adopts high voltage driver IC, so it could be permanently damaged under a wrong power on/off sequence. The suggested LCD power sequence is below:

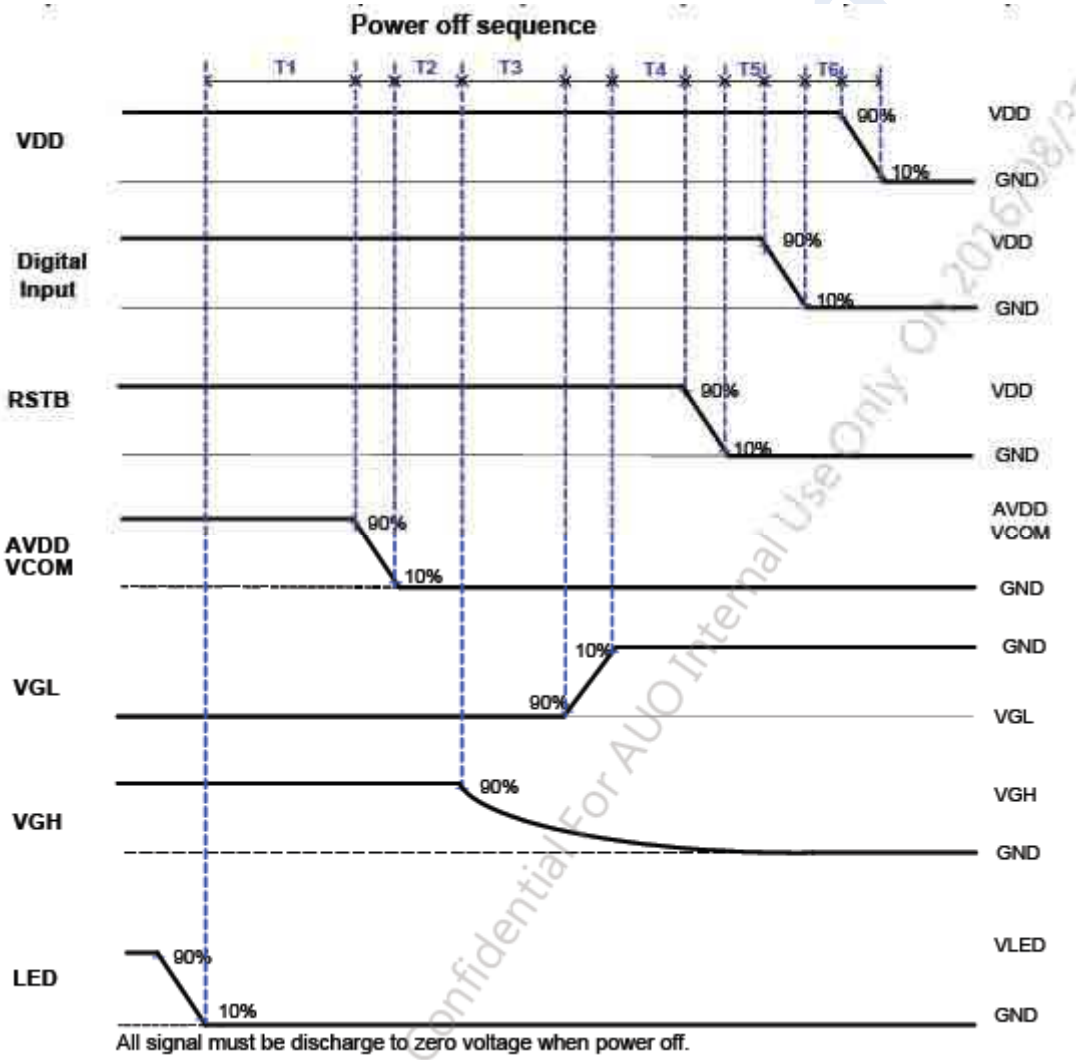
Panel Power on sequence:

Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	--	--	20	ms
T2	1	--	--	ms
T3	1	--	--	ms
T4	134	--	--	ms
T5	1	--	--	ms
T6	1	--	--	ms
T7	16.7	--	--	ms
T8	50	--	--	ms



Panel Power off sequence:

Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	0	--	-	ms
T2	5	--	-	ms
T3	6	--	-	ms
T4	20	--	--	ms
T5	0	--	--	us
T6	0	--	--	us



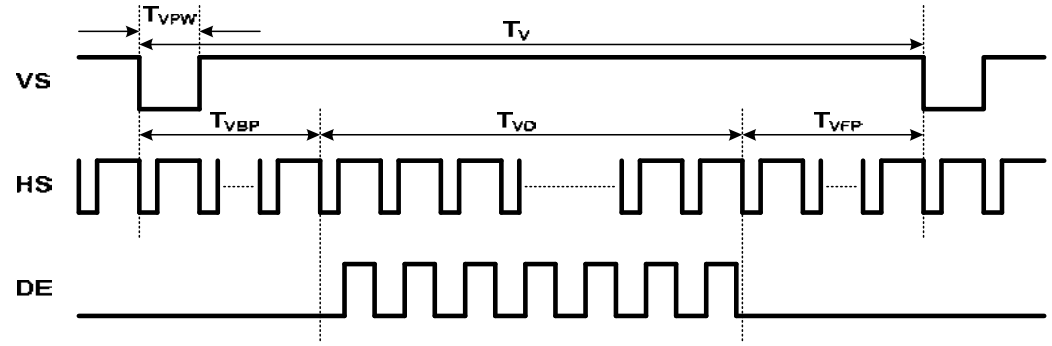
All signal must be discharge to zero voltage when power off.

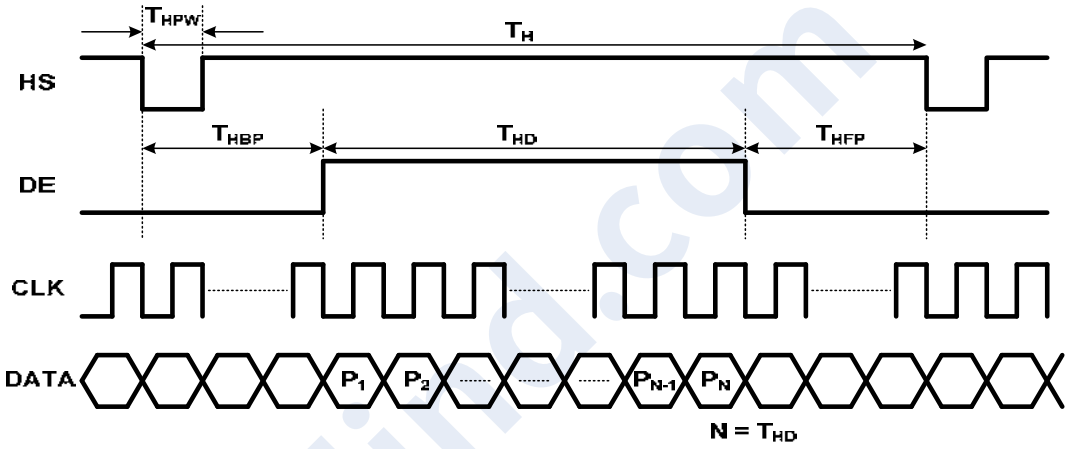
b. Timing Condition

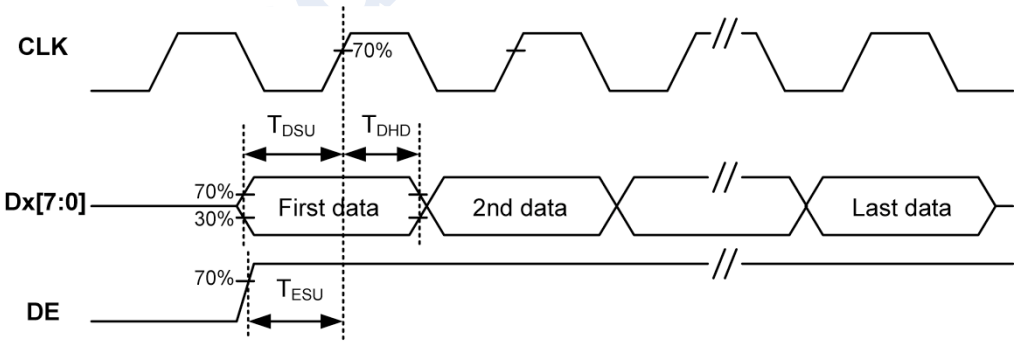
Item	Symbol	Min	Typ	Max	Unit	Remark
Clock frequency	F_{CLK}	33.2	37.0	40.0	MHz	
Vertical display area	T_{VD}		480		H	
Vertical period area	T_V	525	525	530	H	
Vertical blanking area	T_{VB}	45	45	50	H	Note1
Vertical pulse width	T_{VPW}		3		H	
Vertical back porch	T_{VBP}		20		H	
Vertical front porch	T_{VFP}	25	25	30	H	
Horizontal display area	T_{HD}		800		dclk	
Horizontal period area	T_H	1054	1175	1258	dclk	
Horizontal blanking area	T_{HB}	254	375	458	dclk	Note2
Horizontal pulse width	T_{HPW}		3		dclk	
Horizontal back porch	T_{HBP}		48		dclk	
Horizontal front porch	T_{HFP}	206	327	410	dclk	
HS setup time	T_{HSU}	6	-	-	ns	
HS hold time	T_{HHD}	6	-	-	ns	
VS setup time	T_{VSU}	6	-	-	ns	
VS hold time	T_{VHD}	6	-	-	ns	
Data setup time	T_{DSU}	6	-	-	ns	
Data hold time	T_{DHU}	6	-	-	ns	
DE setup time	T_{ESU}	6	-	-	ns	

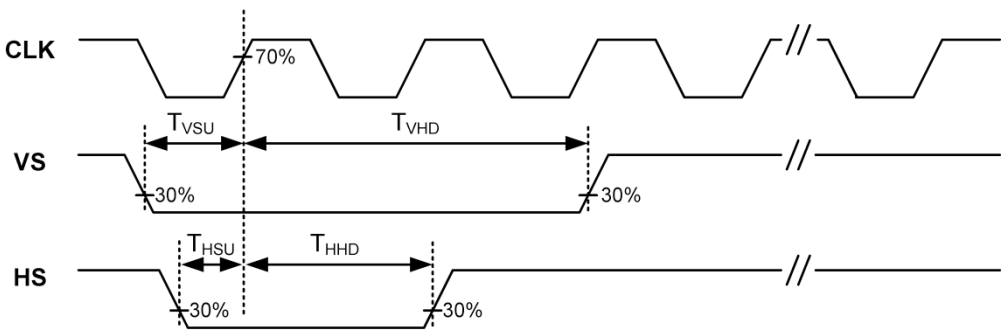
Note1: $T_{VB} = T_V - T_{VD}$
Note2: $T_{HB} = T_H - T_{HD}$

c. Timing Diagram

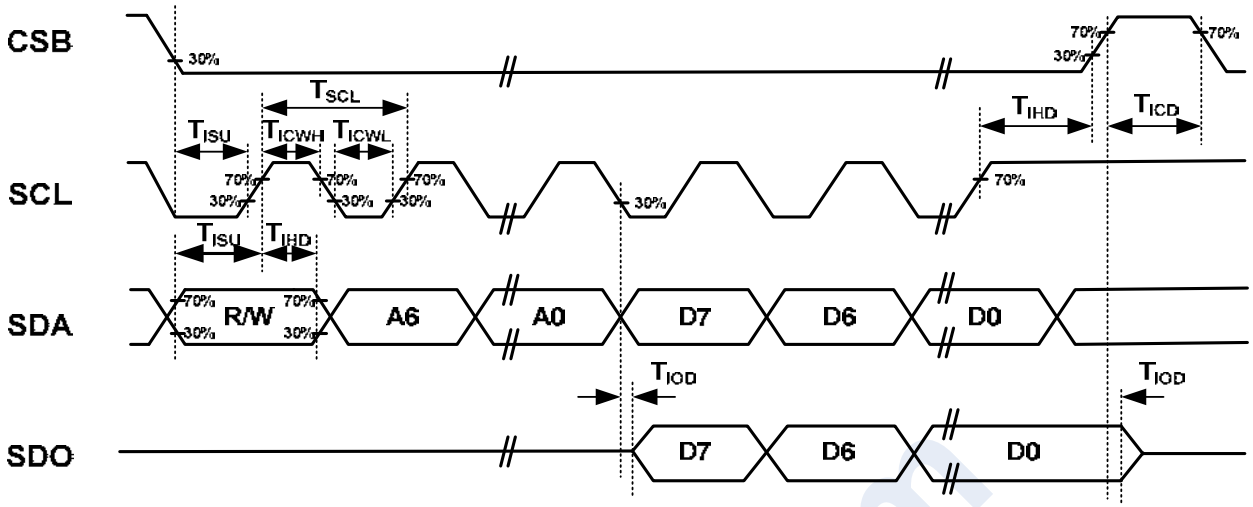








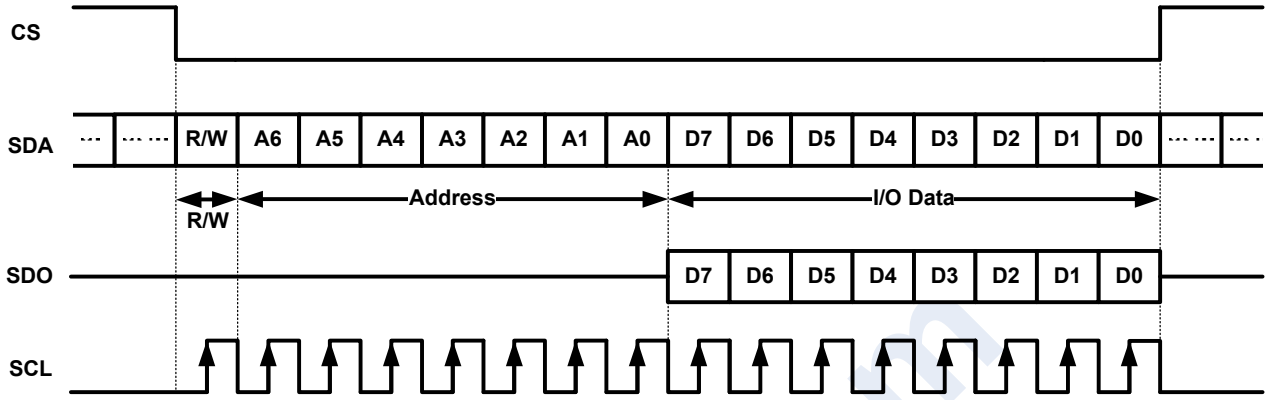
d. Serial control interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
Serial clock	T_{SCL}	330	-	-	ns
SCL HIGH period	T_{ICWH}	150	-	-	ns
SCL LOW period	T_{ICWL}	150	-	-	ns
Serial data setup time	T_{ISU}	120	-	-	ns
Serial data hold time	T_{IHD}	120	-	-	ns
Serial output delay time	T_{IOD}	-	-	30	ns
Chip select distinguish	T_{ICD}	1	-	-	us

e. **Timing chart**

MSB															LSB
R/W	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	Address							I/O Data							



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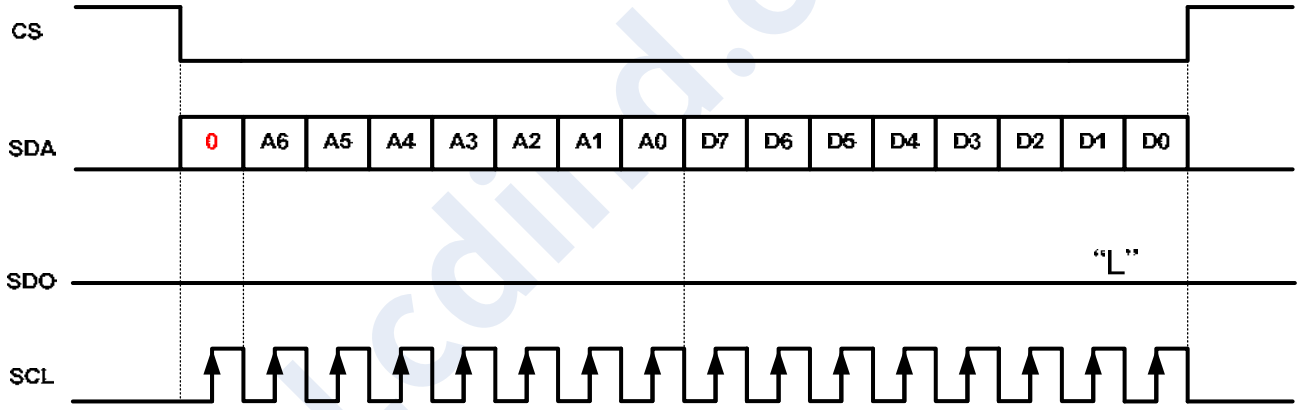

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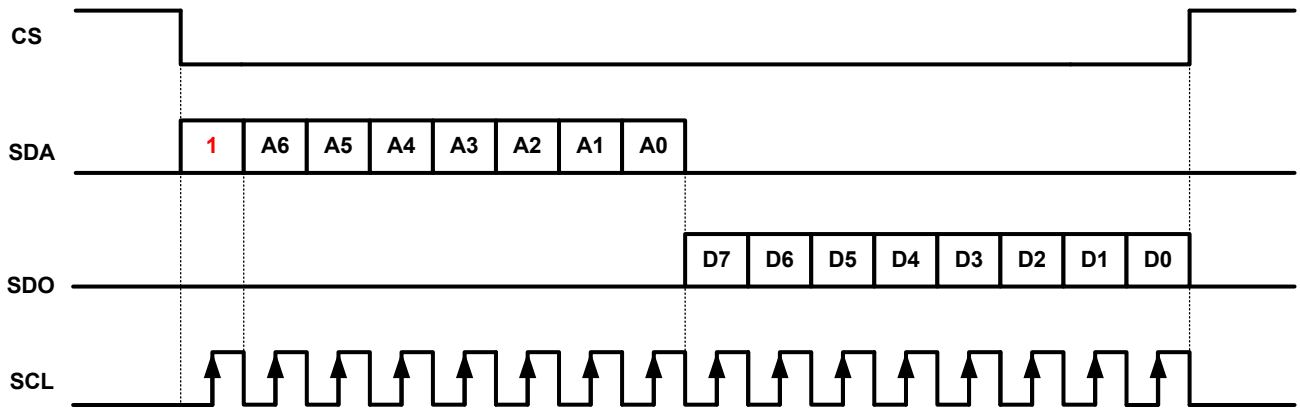


f. Register table (Tentative)

The setting flow can separate to 3 sections. First, determine V1, V9, V10 and V18. Second, choose V2, V8, V11 and V17. Third, choose V3, V7, V12 and V16. Last, choose V4, V5, V6, V13, V14 and V15.

Register address	Register data							
	D7	D6	D5	D4	D3	D2	D1	D0
R01H	0	0	0	0	0	0	GRB(1)	1
R02H	0	1	0	NBW(1)	0	1	SHLR(1)	UPDN(0)
R04H	BGR(0)	BLKINSER(0)	BLKINSER_CK(0)	BWINSER(1)	0	0	LVBIT(1)	LVFMT(1)
R05H	0	0	1	0	BIST(0)	LVD(1)	VSPOL(0)	HSPOL(0)
R08H	1	0	0	1	0	LONG_PLUSE(1)	PRECXH(0)	PRECXG(1)
R09H	BIST_EXTCLK(0)	0	1	1	0	0	0	1
R0AH	VBP[7:0](00010100)							
R0BH	HBP[7:0](00110000)							
R0CH	INV2K_SEL[1:0](11)		INV2K(0)	INV2B(1)	HOEV_WIDTH[3:0](0100)			
R0EH	1	0	0	0	FOEV_WIDTH[3:0](0110)			
R16H	1	1	VDDAG[5:0](11000101)					
R18H	0	0	0	0	Reg_VDDAG[3:0](1011)			
R1EH	REGCTRL[7:0](10101010)							
R20H	1	0	0	V1(R) (1Dh)				
R21H	0	0	0	V2(R) (19h)				
R22H	0	0	0	V3(R) (0Ah)				
R23H	0	0	0	V4(R) (15h)				
R24H	0	0	0	V5(R) (14h)				
R25H	0	0	0	V6(R) (12h)				
R26H	0	0	0	V7(R) (0Eh)				
R27H	0	0	0	V8(R) (01h)				
R28H	0	0	0	V9(R) (13h)				
R29H	0	0	0	V10(R) (11h)				
R2AH	0	0	0	V11(R) (03h)				
R2BH	0	0	0	V12(R) (0Fh)				
R2CH	0	0	0	V13(R) (15h)				
R2DH	0	0	0	V14(R) (16h)				
R2EH	0	0	0	V15(R) (0Fh)				
R2FH	0	0	0	V16(R) (0Dh)				
R30H	0	0	0	V17(R) (1Ch)				
R31H	0	0	0	V18(R) (0Bh)				
R32H	0	0	0	V1(G) (1Dh)				
R33H	0	0	0	V2(G) (19h)				
R34H	0	0	0	V3(G) (0Ah)				
R35H	0	0	0	V4(G) (15h)				
R36H	0	0	0	V5(G) (14h)				
R37H	0	0	0	V6(G) (12h)				
R38H	0	0	0	V7(G) (0Eh)				
R39H	0	0	0	V8(G) (01h)				
R3AH	0	0	0	V9(G) (13h)				
R3BH	0	0	0	V10(G) (11h)				
R3CH	0	0	0	V11(G) (03h)				

R44H	0	0	0	V1(B) (1Dh)
R45H	0	0	0	V2(B) (19h)
R46H	0	0	0	V3(B) (0Ah)
R47H	0	0	0	V4(B) (15h)
R48H	0	0	0	V5(B) (14h)
R49H	0	0	0	V6(B) (12h)
R4AH	0	0	0	V7(B) (0Eh)
R4BH	0	0	0	V8(B) (01h)
R4CH	0	0	0	V9(B) (13h)
R4DH	0	0	0	V10(B) (11h)
R4EH	0	0	0	V11(B) (03h)
R4FH	0	0	0	V12(B) (0Fh)
R50H	0	0	0	V13(B) (15h)
R51H	0	0	0	V14(B) (16h)
R52H	0	0	0	V15(B) (0Fh)
R53H	0	0	0	V16(B) (0Dh)
R54H	0	0	0	V17(B) (1Ch)
R55H	0	0	0	V18(B) (0Bh)

R01h Control Register

Bit	Name	Function
Bit[1]	RSTB	Reset bit RSTB = "0" : The controller is in reset state. RSTB = "1" : Normal operation. (Default)

R02h Control Register

Bit	Name	Function
Bit[4]	NBW	Type of Normally Black/White selection NBW = "1" : Normally Black. (Default)
Bit[1]	SHLR	Horizontal scan direction control. SHLR = "1" : Left to Right. (Default) SHLR = "0" : Right to Left.
Bit[0]	UPDN	Vertical scan direction control. UPDN = "1" : Down to Up. UPDN = "0" : Up to Down. (Default)

R04h Control Register

Bit	Name	Function
Bit[7]	BGR	Color filter arrangement BGR = "0" : RGB color filter. (Default)
Bit[6]	BLKINSER	No_ HV/DE detection. BLKINSER = "0" : Disable. BLKINSER = "1" : Enable. (Default)
Bit[5]	BLKINSER_CK	No_ clock detection. BLKINSER_CK = "0" : Disable. BLKINSER_CK = "1" : Enable. (Default)
Bit[4]	BWINSER	No_ signal data selection. BWINSER = "1" : Black data. (Default) BWINSER = "0" : White data.
Bit[1]	LVBIT	6-bit / 8-bit selection. LVBIT = "1" : 8-bit. (Default)
Bit[0]	LVFMT	LVDS input data format selection. LVFMT = "1" : VESA format. (Default)

R05h Control Register

Bit	Name	Function
Bit[3]	BIST	Normal Operation/BIST pattern select. BIST = "0" : Normal Operation. (Default)
Bit[2]	LVD	LOW Voltage Detection. LVD = "1" : Function on. (Default)
Bit[1]	VSPOL	VSYNC polarity. VSPOL = "0" : Negative polarity. (Default)
Bit[0]	HSPOL	HSYNC polarity. HSPOL = "0" : Negative polarity. (Default)

R08h Control Register

Bit	Name	Function
Bit[2]	LONG_PULSE	Long start pulse enable. LONG_PULSE = "1" : Long start pulse. (Default)
Bit[1]	PREXH	Tri-gate pre-charge duration. PREXH = "0" : 2 x 1/3H duration. (Default)
Bit[0]	PRECHG	Tri-gate pre-charge function. PRECHG = "1" : Enable. (Default)

R09h Control Register

Bit	Name	Function
Bit[7]	BIST_EXTCLK	External BIST clock select BIST_EXTCLK = "0" : Internal clock. (Default)

R0Ah Control Register

Bit	Name	Function
Bit[7:0]	VBP	Vertical Back Porch Select. VBP = 3~127, When PRECHG = H, please make sure there are enough V-blanking area to accommodate pre-charge timing.

R0Bh Control Register

Bit	Name	Function
Bit[7:0]	HBP	Horizontal Back Porch Select. HBP = 12~178

R0Ch Control Register

Bit	Name	Function
Bit[7:6]	INV2K_SEL	INV2K VS selection. INV2K_SEL = 256 VS. (Default)
Bit[5]	INV2K	Polarity inversion change after 256 VS. INV2K = "H" : Enable. (Default)
Bit[4]	INV2B	2-Frame polarity inversion. INV2B = "H" : Disable. (Default)
Bit[3:0]	HOEV_WIDTH	OE pulse edge control. HOEV_WIDTH = 4h : 39 DCLK. (Default)

R0Eh Control Register

Bit	Name	Function
Bit[3:0]	FOEV_WIDTH	OE pulse edge control. FOEV_WIDTH = 6h : 111 DCLK. (Default)

R16h Control Register

Bit	Name	Function						
Bit[5:0]	VDDAG	Voltage setting of VDDAG						
		VDDAG[5:0]						VDDAG(V)
		1	1	1	1	1	1	11.9327
		1	1	1	1	1	0	11.9471
		1	1	1	1	0	1	11.9614
		1	1	1	1	0	0	11.9759
		1	1	1	0	1	1	11.9903
		1	1	1	0	1	0	12.0048
		1	1	1	0	0	1	12.0194
		1	1	1	0	0	0	12.0339
		1	1	0	1	1	1	12.0485
		1	1	0	1	1	0	12.0632
		1	1	0	1	0	1	12.0779
		1	1	0	1	0	0	12.0926
		1	1	0	0	1	1	12.1073
		1	1	0	0	1	0	12.1221
		1	1	0	0	0	1	12.1369
		1	1	0	0	0	0	12.1518
		1	0	1	1	1	1	12.1667
		1	0	1	1	1	0	12.1816
		1	0	1	1	0	1	12.1966
		1	0	1	1	0	0	12.2116
		1	0	1	0	1	1	12.2266
		1	0	1	0	1	0	12.2417
		1	0	1	0	0	1	12.2568
		1	0	1	0	0	0	12.2719
		1	0	0	1	1	1	12.2871
		1	0	0	1	1	0	12.3024
		1	0	0	1	0	1	12.3176
		1	0	0	1	0	0	12.3329
		1	0	0	0	1	1	12.3483
		1	0	0	0	1	0	12.3636

		1	0	0	0	0	1	12.3791
		1	0	0	0	0	0	12.3945
		0	**0**	**0**	**0**	**0**	**0**	**12.41**
		0	0	0	0	0	1	12.4255
		0	0	0	0	1	0	12.4411
		0	0	0	0	1	1	12.4567
		0	0	0	1	0	0	12.4724
		0	0	0	1	0	1	12.4881
		0	0	0	1	1	0	12.5038
		0	0	0	1	1	1	12.5195
		0	0	1	0	0	0	12.5354
		0	0	1	0	0	1	12.5512
		0	0	1	0	1	0	12.5671
		0	0	1	0	1	1	12.583
		0	0	1	1	0	0	12.599
		0	0	1	1	0	1	12.615
		0	0	1	1	1	0	12.631
		0	0	1	1	1	1	12.6471
		0	1	0	0	0	0	12.6633
		0	1	0	0	0	1	12.6794
		0	1	0	0	1	0	12.6957
		0	1	0	0	1	1	12.7119
		0	1	0	1	0	0	12.7282
		0	1	0	1	0	1	12.7445
		0	1	0	1	1	0	12.7609
		0	1	0	1	1	1	12.7773
		0	1	1	0	0	0	12.7938
		0	1	1	0	0	1	12.8103
		0	1	1	0	1	0	12.8269
		0	1	1	0	1	1	12.8435
		0	1	1	1	0	0	12.8601
		0	1	1	1	0	1	12.8768
		0	1	1	1	1	0	12.8935
		0	1	1	1	1	1	12.9103

R18h Control Register

Bit	Name	Function
Bit[3:0]	Reg_VDDAG	Enable VDDAG register. Set "1011" to enable VDDAG[5:0].

R1Eh Control Register

Bit	Name	Function
Bit[7:0]	REGCTRL	Register control enable. REGCTRL = AAh.(Default)

R20h Gamma Register

Bit	Name	Function
Bit[7]	Reg_Gam	Gamma register enable. Reg _ Gam="0" , disable gamma registers. (Default) Reg _ Gam="1", enable gamma registers. Note:set Reg _ Gam to "1" for adjusting gamma. Otherwise, gamma registers will keep the default value setting .
Bit[0:4]	V1(R)	V1(R) = GMAH x (169 + $(V1R)_D$) / 200

R21h Gamma Register

Bit	Name	Function
Bit[0:4]	V2(R)	V2(R) = V9(R) + (V1(R) - V9(R)) x (69 + $(V2R)_D$) / 100

R22h Gamma Register

Bit	Name	Function
Bit[0:4]	V3(R)	V3(R) = V8(R) + (V2(R) – V8(R)) x (59 + $(V3R)_D$) / 100

R23h Gamma Register

Bit	Name	Function
Bit[0:4]	V4(R)	V4(R) = V7(R) + (V3(R) – V7(R)) x (55 + $(V4R)_D$) / 100

R24h Gamma Register

Bit	Name	Function
Bit[0:4]	V5(R)	V5(R) = V7(R) + (V3(R) – V7(R)) x (26 + $(V5R)_D$) / 100

R25h Gamma Register

Bit	Name	Function
Bit[0:4]	V6(R)	V6(R) = V7(R) + (V3(R) – V7(R)) x (3 + $(V6R)_D$) / 100

R26h Gamma Register

Bit	Name	Function
Bit[0:4]	V7(R)	V7(R) = V8(R) + (V2(R) - V8(R)) x (8 + $(V7R)_D$) / 100

R27h Gamma Register

Bit	Name	Function
Bit[0:4]	V8(R)	V8(R) = V9(R) + (V1(R) - V9(R)) x $(V8R)_D$/ 100

R28h Gamma Register

Bit	Name	Function
Bit[0:4]	V9(R)	V9(R) = GMAH x (95 + $(V9R)_D$) / 200

R29h Gamma Register

Bit	Name	Function
Bit[0:4]	V10(R)	V10(R) = GMAH x (118 - $(V10R)_D$) / 200

R2Ah Gamma Register

Bit	Name	Function
Bit[0:4]	V11(R)	V11(R) = V10(R) - (V10(R) – V18(R)) x $(V11R)_D$/ 100

R2Bh Gamma Register

Bit	Name	Function
Bit[0:4]	V12(R)	V12(R) = V11(R) - (V11(R) – V17(R)) x (8 + $(V12R)_D$) / 100

R2Ch Gamma Register

Bit	Name	Function
Bit[0:4]	V13(R)	V13(R) = V12(R) - (V12(R) – V16(R)) x $(V13R)_D$/ 100

R2Dh Gamma Register

Bit	Name	Function
Bit[0:4]	V14(R)	V14(R) = V12(R) - (V12(R) – V16(R)) x (26 + $(V14R)_D$) / 100

Bit	Name	Function
Bit[0:4]	V15(R)	V15(R) = V12(R) - (V12(R) – V16(R)) x (62 + $(V15R)_D$) / 100

R2Fh Gamma Register

Bit	Name	Function
Bit[0:4]	V16(R)	V16(R) = V11(R) - (V11(R) – V17(R)) x (57 + $(V16R)_D$) / 100

R30h Gamma Register

Bit	Name	Function
Bit[0:4]	V17(R)	V17(R) = V10(R) - (V10(R) – V18(R)) x (69 + $(V17R)_D$) / 100

R31h Gamma Register

Bit	Name	Function
Bit[0:4]	V18(R)	V18(R) = GMAH x (31 - $(V18R)_D$) / 200

Register command flow

No.	Register address	Register data	Setting value	Remark
1	R1EH	10101010	0XAA	Note 1.
2	R18H	00001011	0X0B	
3	R01H	00000011	0X03	
4	R02H	01010110	0X56	
5	R04H	00110011	0X33	Note 2.
6	R05H	00100100	0X24	
7	R08H	10010101	0X95	
8	R09H	00110001	0X31	
9	R0AH	00010100	0X14	
10	R0BH	00110000	0X30	
11	R0CH	11010100	0XD4	
12	R0EH	10000110	0X86	
13	R16H	11100010	0XE2	
14	R20H	00011111	0X1F	
15	R32H	00011111	0X1F	
16	R44H	00011111	0X1F	
17	R28H	00010000	0X10	
18	R3AH	00010000	0X10	
19	R4CH	00010000	0X10	
20	R29H	00010100	0X14	
21	R3BH	00010100	0X14	
22	R4DH	00010100	0X14	
23	R31H	00010010	0X12	
24	R43H	00010010	0X12	
25	R55H	00010010	0X12	
26	R21H	00010111	0X17	
27	R33H	00010111	0X17	
28	R45H	00010111	0X17	
29	R27H	00000010	0X02	
30	R39H	00000010	0X02	
31	R4BH	00000010	0X02	
32	R2AH	00000010	0X02	
33	R3CH	00000010	0X02	
34	R4EH	00000010	0X02	

35	R30H	00010101	0X15	
36	R42H	00010101	0X15	
37	R54H	00010101	0X15	
38	R22H	00001010	0X0A	
39	R34H	00001010	0X0A	
40	R46H	00001010	0X0A	
41	R26H	00001111	0X0F	
42	R38H	00001111	0X0F	
43	R4AH	00001111	0X0F	
44	R2BH	00010000	0X10	
45	R3DH	00010000	0X10	
46	R4FH	00010000	0X10	
47	R2FH	00001101	0X0D	
48	R41H	00001101	0X0D	
49	R53H	00001101	0X0D	
50	R23H	00010100	0X14	
51	R35H	00010100	0X14	
52	R47H	00010100	0X14	
53	R24H	00010100	0X14	
54	R36H	00010100	0X14	
55	R48H	00010100	0X14	
56	R25H	00010000	0X10	
57	R37H	00010000	0X10	
58	R49H	00010000	0X10	
59	R2CH	00010101	0X15	
60	R3EH	00010101	0X15	
61	R50H	00010101	0X15	
62	R2DH	00010110	0X16	
63	R3FH	00010110	0X16	
64	R51H	00010110	0X16	
65	R2EH	00001111	0X0F	
66	R40H	00001111	0X0F	
67	R52H	00001111	0X0F	

F. Optical specifications (Note 1, 2)

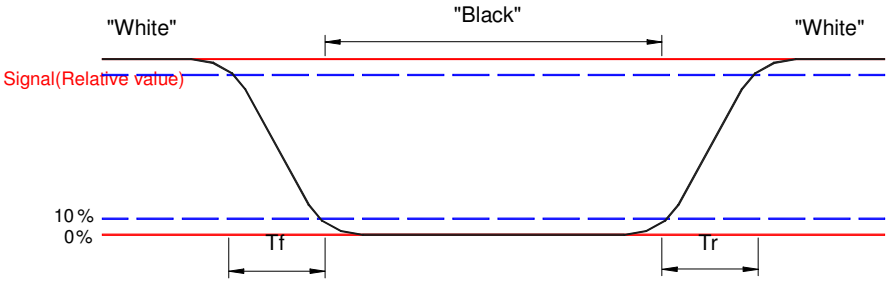
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall	 Tr Tf	θ =0°	 - -	 9 11	 - -	ms	Note 3
Contrast ratio	CR	θ =0°	800	1000	-		Note 4, 5, 6
Viewing Angle Top Bottom Left Right		CR≧100	 70 70 70 70	 80 80 80 80		deg.	Note 7, 8
Brightness	Y_L	θ =0°	450	500	600	cd/m	Note 1,2,9
White Chromaticity	X	θ =0°	0.248	0.298	0.348		Note 8
	Y	θ =0°	0.271	0.321	0.371		
Red Chromaticity	X						
	Y						
Green Chromaticity	X						
	Y						
Blue Chromaticity	X						
	Y						
Uniformity		9-point, θ=0°	80	-	-	%	Note 10

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25°C, and backlight current I_L=80 mA

Note 2: To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter SR-3, after 10 minutes operation and warm up 30 minutes.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



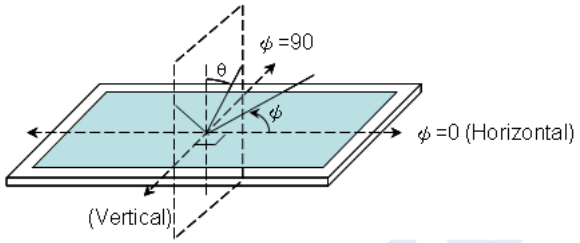
Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25℃.

$$\text{Contrastratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5. Contrast ratio is calculated with the following formula.

Note 6. White : RGB data = '' 11111111''
Black : RGB data = ''00000000"
100% transmission is defined as the transmission of LCD panel when all the inputterminals of Module are electrically opened.

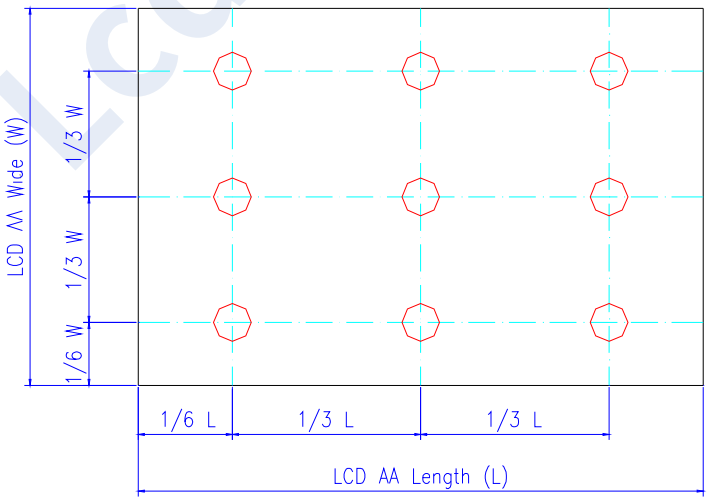
Note 7. Definition of viewing angle: refer to figure as below.



Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.
If user finds panel that is out of color range, AUO will proceed to RMA (Return Material Authorisation) Process to exchange panel piece by piece without the failure rate counting.

Note 9. Brightness is measured at the center of the display with white pattern in 80mA

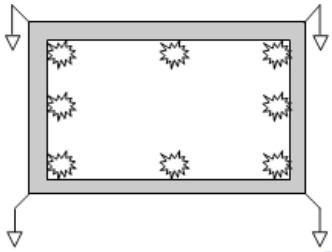
Note 10. Luminance Uniformity is defined as following within the 9 measurements (L1~L9),
Luminance Uniformity(%) =Minimum luminance(brightness)/Maximum luminance(brightness)

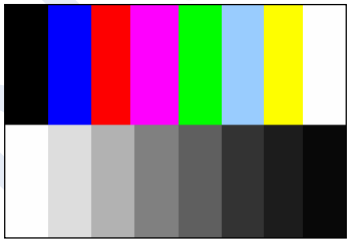


G. Reliability Test Items (Note 2)

No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 70℃	240Hrs	Note1
2	Low temperature storage	Ta= -20℃	240Hrs	
3	High temperature operation	Ta= 60℃	240Hrs	
4	Low temperature operation	Ta= -10℃	240Hrs	Note1, 3
5	High temperature and high humidity	Ta= 60℃, 90% RH	240Hrs	Operation
6	Heat shock	-10℃~60℃ /100 cycles 1Hrs/cycle		Non-operation
7	Electrostatic discharge	Contact = ± 8 kV, class B (R=330Ω,C=150pF) Air = ± 15 kV, class B (R=330Ω,C=150pF)		Operation (Note 4)

Note 1: Ta: Ambient temperature.
Note 2: In the standard condition, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.
Note 3: Short time operation between -40℃~-30℃ doesn't provide full performance but a correct image on the LCD. The LCD is guaranteed to suffer no permanent damage.
Note 4: Test techniques follow IEC61000-4-2 standard. Test points and pattern as below.





H. Packing

T.B.D.